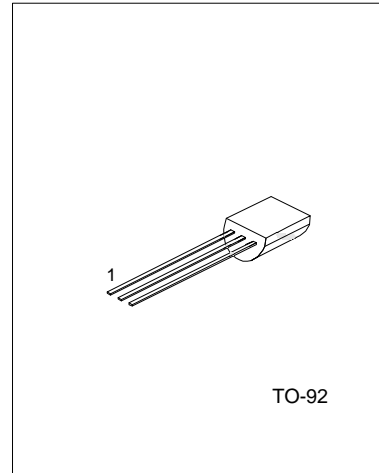


DESCRIPTION

The UTC BT169 is glass passivated, sensitive gate thyristors in a plastic envelope, intended for use in general purpose switching and phase control applications. These devices are intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.



1:CATHODE 2:GATE 3:ANODE

QUICK REFERENCE DATA

PARAMETER	SYMBOL	MAX(B)	MAX(D)	MAX(E)	MAX(G)	UNIT
Repetitive peak off-state voltages	V <sub>DRM</sub> , V <sub>RRM</sub>	200	400	500	600	V
Average on-state current	I <sub>T(AV)</sub>	0.5	0.5	0.5	0.5	A
RMS on-state current	I <sub>T(RMS)</sub>	0.8	0.8	0.8	0.8	A
Non-repetitive peak on-state current	I <sub>TSM</sub>	8	8	8	8	A

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNIT
Repetitive peak off-state voltages :	V <sub>DRM</sub> , V <sub>RRM</sub>			B:200 D:400 E:500 G:600	V
Average on-state current	I <sub>T(AV)</sub>	Half sine wave; T <sub>lead</sub> ≤ 83°C		0.5	A
RMS on-state current	I <sub>T(RMS)</sub>	All conduction angles		0.8	A
Non-repetitive peak on-state current	I <sub>TSM</sub>	t = 10ms t = 8.3ms half sine wave; T <sub>j</sub> = 25°C prior to surge		8 9	A
I <sup>2</sup> t for fusing	I <sup>2</sup> t	t = 10ms		0.32	A <sup>2</sup> S
Repetitive rate of rise of on-state current after triggering	DI <sub>T</sub> /dt	I <sub>TM</sub> = 2A; I <sub>G</sub> = 10mA; di <sub>G</sub> /dt = 100mA/μs		50	A/μs
Peak gate current	I <sub>GM</sub>			1	A
Peak gate voltage	V <sub>GM</sub>			5	V
Peak reverse gate voltage	V <sub>RGM</sub>			5	V

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNIT
Peak gate power	PGM			2	W
Average gate power	PG(AV)	Over any 20 ms period		0.1	W
Storage temperature	Tstg		-40	150	°C
Operating junction temperature	Tj			125	°C

## THERMAL RESISTANCES

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Thermal resistance junction to lead	Rth j-lead				60	K/W
Thermal resistance junction to ambient	Rth j-a	pcb mounted; lead length=4mm		150		K/W

## ELECTRICAL CHARACTERISTICS (Tj=25°C unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
STATIC						
Gate trigger current	IGT	V <sub>D</sub> =12V; I <sub>T</sub> =10mA; gate open circuit		50	200	μA
Latching current	IL	V <sub>D</sub> =12V; I <sub>GT</sub> =0.5mA; R <sub>GK</sub> =1kΩ		2	6	mA
Holding current	IH	V <sub>D</sub> =12V; I <sub>GT</sub> =0.5mA; R <sub>GK</sub> =1kΩ		2	5	mA
On-state voltage	V <sub>T</sub>	I <sub>T</sub> =1A		1.2	1.35	V
Gate trigger voltage	V <sub>GT</sub>	V <sub>D</sub> =12V; I <sub>T</sub> =10mA; gate open circuit		0.5	0.8	V
		V <sub>D</sub> =V <sub>DRM(max)</sub> ; I <sub>T</sub> =10mA; T <sub>j</sub> =125°C; gate open circuit	0.2	0.3		
Off-state leakage current	I <sub>D</sub> , I <sub>R</sub>	V <sub>D</sub> =V <sub>DRM(max)</sub> ; V <sub>R</sub> =V <sub>R<sub>RRM</sub>(max)</sub> ; T <sub>j</sub> =125°C; R <sub>GK</sub> =1kΩ		0.05	0.1	mA
DYNAMIC						
Critical rate of rise of off-state voltage	dV <sub>D</sub> /dt	V <sub>DM</sub> =67% V <sub>DRM(max)</sub> ; T <sub>j</sub> =125°C; exponential waveform; R <sub>GK</sub> =1kΩ		25		V/μs
Gate controlled turn-on time	t <sub>gt</sub>	I <sub>TM</sub> =2A; V <sub>D</sub> =V <sub>DRM(max)</sub> ; I <sub>G</sub> =10mA; dI <sub>G</sub> /dt=0.1A/μs		2		μs
Circuit commutated turn-off time	t <sub>q</sub>	V <sub>D</sub> =67% V <sub>DRM(max)</sub> ; T <sub>j</sub> =125°C; I <sub>TM</sub> =1.6A; V <sub>R</sub> =35V; dI <sub>TM</sub> /dt=30A/μs; V <sub>D</sub> /dt=2V/μs; R <sub>GK</sub> =1kΩ		100		μs

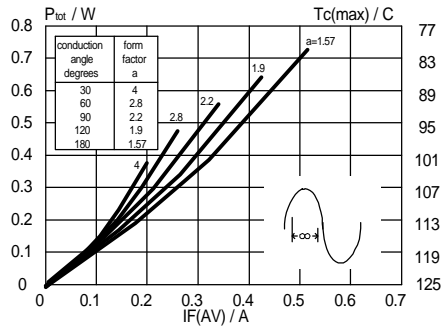


FIG.1 Maximum on-state dissipation,  $P_{tot}$ , versus average on-state current,  $I_{T(AV)}$ , where  $a = \text{form factor} = I_{T(RMS)} / I_{T(AV)}$

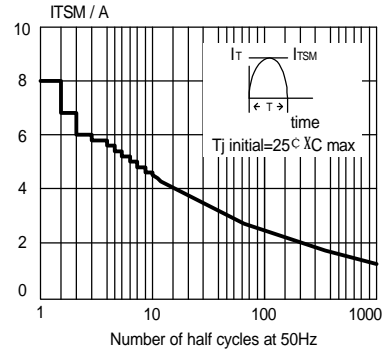


FIG.4 Maximum permissible non-repetitive peak on-state current  $I_{TSM}$ , versus number of cycles, for sinusoidal currents,  $f = 50\text{Hz}$ .

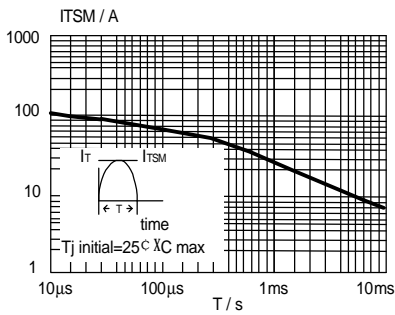


FIG.2 Maximum permissible non-repetitive peak on-state current  $I_{TSM}$ , versus pulse width  $t_p$ , for sinusoidal currents,  $t_p \leq 10\text{ms}$ .

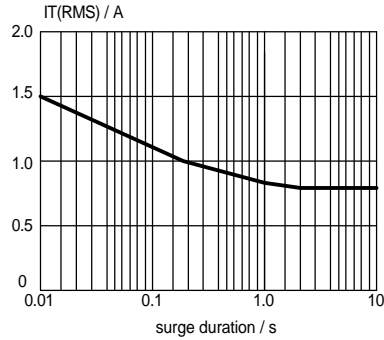


FIG.5 Maximum permissible repetitive rms on-state current  $I_{T(RMS)}$ , versus surge duration, for sinusoidal currents,  $f = 50\text{Hz}$ ;  $T_{lead} \leq 83^\circ\text{C}$

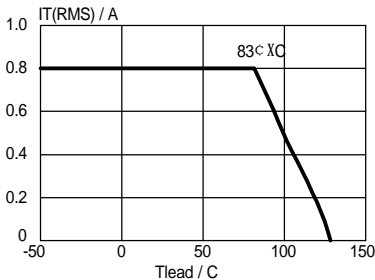


FIG.3 Maximum permissible rms current  $I_{T(RMS)}$ , versus lead temperature,  $T_{lead}$

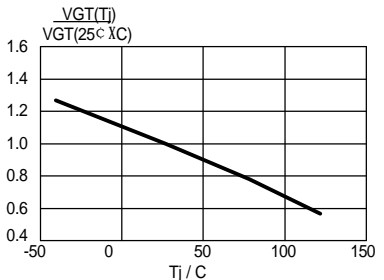


FIG.6 Normalised gate trigger voltage  $V_{GT(I_T)} / V_{GT(25^\circ\text{C})}$ , versus junction temperature  $T_j$

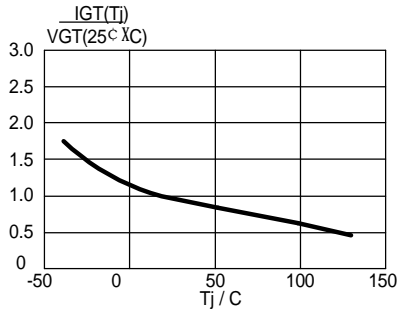


FIG.7 Normalised gate trigger current  $I_{GT}(T_j)/I_{GT}(25^\circ\text{C})$ , versus junction temperature  $T_j$

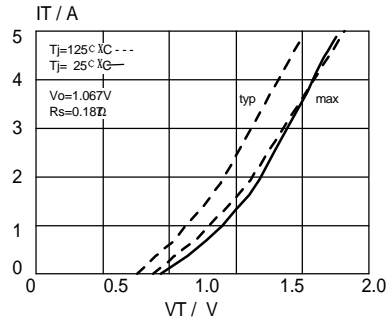


FIG.10 Typical and maximum on-state characteristic.

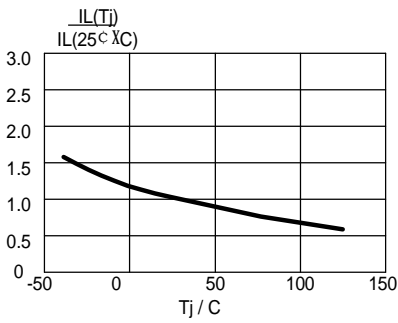


FIG.8 Normalised latching current  $I_L(T_j)/I_L(25^\circ\text{C})$ , versus junction temperature  $T_j$ ,  $R_{GK} = 1\text{K}\Omega$

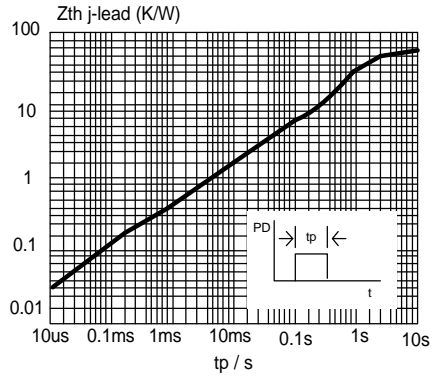


FIG.11 Transient thermal impedance  $Z_{th \text{ j-lead}}$ , versus pulse width  $t_p$ .

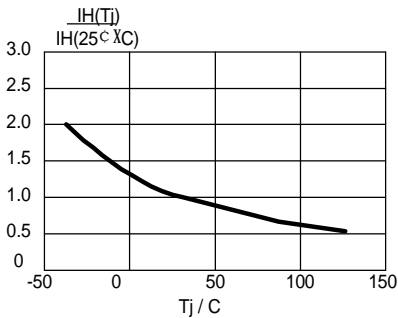


FIG.9 Normalised holding current  $I_H(T_j)/I_H(25^\circ\text{C})$ , versus junction temperature  $T_j$ ,  $R_{GK} = 1\text{K}\Omega$

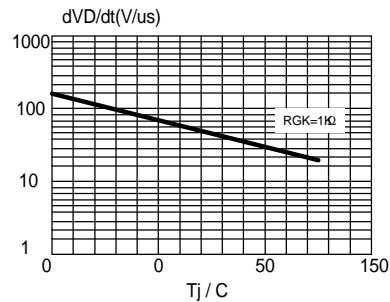


FIG.12 Typical, critical rate of rise of off-state voltage,  $dV/dt$  versus junction temperature  $T_j$ .